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Cancel claims 1-27.

28. (New) A serial stream interface for combining a master serial data stream comprising a sequence of N-bit master data packets and a slave serial data stream comprising a sequence of N-bit slave data packets, said serial stream interface comprising:

a slave input interface capable of converting said slave serial data stream to an N-bit slave parallel output that outputs each of said N-bit slave data packets in parallel;

a source selection circuit capable of receiving an N-bit master parallel output from a first master data source and said N-bit slave parallel output and outputting a selected one of said N-bit master parallel output and said N-bit slave parallel output; and

a serialization circuit capable of receiving said selected one of said N-bit master parallel output and said N-bit slave parallel output and converting said selected one of said N-bit master parallel output and said N-bit slave parallel output to an output serial data stream.

29. (New) The serial stream interface as set forth in Claim 28, wherein said slave input interface comprises a slave buffer having a serial input for receiving said slave serial data stream and

an N-bit slave parallel output for outputting each of said N-bit slave data packets, wherein said slave buffer stores said each N-bit slave data packet using at least one slave timing signal associated with said slave serial data stream.

30. (New) The serial stream interface as set forth in Claim 29, wherein each bit in said each N-bit slave data packet stored in said slave buffer becomes available in said N-bit slave parallel output substantially concurrently with storage of said each bit in said slave buffer.

31. (New) The serial stream interface as set forth in Claim 29, wherein said slave buffer is a first-in, first-out (FIFO) device.

32. (New) The serial stream interface as set forth in Claim 29, wherein said slave buffer is a 1xN-bit random access memory (RAM).

33. (New) A radio frequency (RF) receiver comprising:

a receiver front-end circuit capable of receiving an incoming RF signal from an antenna and generating an amplified RF output signal;

demodulation circuitry capable of demodulating said amplified RF output signal and generating a plurality of baseband serial data streams;

a serial stream interface capable of receiving said plurality of baseband serial data streams

and combining a master serial data stream comprising a sequence of N-bit master data packets and a slave serial data stream comprising a sequence of N-bit slave data packets, said serial stream interface comprising:

a slave input interface capable of converting said slave serial data stream to an N-bit slave parallel output that outputs each of said N-bit slave data packets in parallel;

a source selection circuit capable of receiving an N-bit master parallel output from a first master data source and said N-bit slave parallel output and outputting a selected one of said N-bit master parallel output and said N-bit slave parallel output; and

a serialization circuit capable of receiving said selected one of said N-bit master parallel output and said N-bit slave parallel output and converting said selected one of said N-bit master parallel output and said N-bit slave parallel output to an output serial data stream.; and

a digital signal processor capable of receiving and processing said output serial data stream.

34. (New) The RF receiver as set forth in Claim 33, wherein said slave input interface comprises a slave buffer having a serial input for receiving said slave serial data stream and an N-bit slave parallel output for outputting each of said N-bit slave data packets, wherein said slave buffer stores said each N-bit slave data packet using at least one slave timing signal associated with said slave serial data stream.

35. (New) The RF receiver as set forth in Claim 34, wherein each bit in said each N-bit slave data packet stored in said slave buffer becomes available in said N-bit slave parallel output substantially concurrently with storage of said each bit in said slave buffer.

36. (New) The RF receiver as set forth in Claim 34, wherein said slave buffer is a first-in, first-out (FIFO) device.

37. (New) The RF receiver as set forth in Claim 34, wherein said slave buffer is a 1xN-bit random access memory (RAM).

38. (New) A radio frequency (RF) transmitter comprising:

a serial stream interface capable of receiving a plurality of baseband serial data streams from a plurality of baseband data sources and combining a master serial data stream comprising a sequence of N-bit master data packets and a slave serial data stream comprising a sequence of N-bit slave data packets, said serial stream interface comprising:

a slave input interface capable of converting said slave serial data stream to an N-bit slave parallel output that outputs each of said N-bit slave data packets in parallel;

a source selection circuit capable of receiving an N-bit master parallel output from a first master data source and said N-bit slave parallel output and outputting a selected one of said N-bit master parallel output and said N-bit slave parallel output; and

a serialization circuit capable of receiving said selected one of said N-bit master parallel output and said N-bit slave parallel output and converting said selected one of said N-bit master parallel output and said N-bit slave parallel output to an output serial data stream.; and

a digital signal processor capable of receiving and processing said output serial data stream; and

an RF modulation circuit capable of receiving a processed output data stream from said digital signal processor and up-converting said output processed data stream to produce a modulated RF signal.

39. (New) The RF transmitter as set forth in Claim 38, wherein said slave input interface comprises a slave buffer having a serial input for receiving said slave serial data stream and an N-bit slave parallel output for outputting each of said N-bit slave data packets, wherein said slave buffer stores said each N-bit slave data packet using at least one slave timing signal associated with said slave serial data stream.

40. (New) The RF transmitter as set forth in Claim 39, wherein each bit in said each N-bit slave data packet stored in said slave buffer becomes available in said N-bit slave parallel output substantially concurrently with storage of said each bit in said slave buffer.

41. (New) The RF transmitter as set forth in Claim 39, wherein said slave buffer is a first-in, first-out (FIFO) device.

42. (New) The RF transmitter as set forth in Claim 39, wherein said slave buffer is a 1xN-bit random access memory (RAM).

43. (New) A method for combining a master serial data stream comprising a sequence of N-bit master data packets and a slave serial data stream comprising a sequence of N-bit slave data packets, the method comprising the steps of:

converting the slave serial data stream to an N-bit slave parallel output in which each of the N-bit slave data packets is output in parallel;

receiving an N-bit master parallel output from a first master data source;

selecting one of the N-bit master parallel output and the N-bit slave parallel output; and

converting the selected one of the N-bit master parallel output and the N-bit slave parallel output to an output serial data stream.

44. (New) The method as set forth in Claim 43, wherein the step of converting the slave serial data stream comprising the sub-steps of:

receiving the slave serial data stream; and

storing each of the N-bit slave data packets in a slave buffer using at least one slave timing

signal associated with the slave serial data stream.

45. (New) The method as set forth in Claim 44, wherein the each bit in the each N-bit slave data packet stored in the slave buffer becomes available in the N-bit slave parallel output substantially concurrently with storage of the each bit in the slave buffer.

46. (New) The method as set forth in Claim 44, wherein the slave buffer is a first-in, first-out (FIFO) device.

47. (New) The method as set forth in Claim 44, wherein the slave buffer is a 1xN-bit random access memory (RAM).